IN THE CLAIMS

Please amend the claims as follows:

1. (Cancelled)

2. (Currently Amended) A capacitor comprising:

at least four conductive layers embedded in a dielectric, wherein the at least four conductive layers includes a first plurality of conductive layers interlaced with a second plurality of conductive layers; and

a plurality of vias coupling the at least four conductive layers to a plurality of connection sites, wherein the plurality of vias includes a first set of vias and a second set of vias, and the first set of vias couples the first plurality of conductive layers to a first plurality of connection sites on at least two surfaces of the capacitor, and the first set of vias extends through openings in and is electrically isolated from the second plurality of conductive layers, and the second set of vias couples the second plurality of conductive layers to a second plurality of connection sites on the at least two surfaces, and the second set of vias extends through openings in and is electrically isolated from the first plurality of conductive layers, and wherein the capacitor has a thickness of between about .5 millimeter and about 1 millimeter.

3. (Original) The capacitor of claim 2, wherein the capacitor has a capacitance of between about 20 and about 30 microfarads.

4. (Cancelled)

5 (Currently Amended) A capacitor comprising:

at least four conductive layers embedded in a dielectric, wherein the at least four conductive layers includes a first plurality of conductive layers interlaced with a second plurality of conductive layers; and

a plurality of vias coupling the at least four conductive layers to a plurality of connection sites on at least two surfaces of the capacitor, wherein the plurality of vias includes a first set of

vias and a second set of vias, and the first set of vias couples the first plurality of conductive layers to a first plurality of connection sites on the at least two surfaces of the capacitor, and the first set of vias extends through openings in and is electrically isolated from the second plurality of conductive layers, and the second set of vias couples the second plurality of conductive layers to a second plurality of connection sites on the at least two surfaces, and the second set of vias extends through openings in and is electrically isolated from the first plurality of conductive layers, and wherein the plurality of vias are plated through holes.

6. (Currently Amended) A capacitor comprising:

a plurality of first conductive layers, each of the plurality of first conductive layers formed on a first dielectric sheet;

a plurality of second conductive layers, each of the plurality of second conductive layers formed on a second dielectric sheet, and the plurality of second conductive layers interlaced with the plurality of first conductive layers;

a pair of dielectric sheets formed from barium titanate, each of the pair of dielectric sheets having a thickness slightly greater than about 7 microns, for providing a pair of substantially rigid outer surfaces for the plurality of second conductive layers interlaced with the plurality of first conductive layers, each of the pair of substantially rigid outer surfaces having a plurality of connection sites operable for coupling the capacitor to a substrate using a controlled collapse chip connection (C4); and

a plurality of vias coupling the plurality of first conductive layers and the plurality of second conductive layers to at least two of the plurality of connection sites.

7. (Original) The capacitor of claim 6, wherein each of the plurality of first conductive layers is fabricated from a tungsten paste.

8. (Original) The capacitor of claim 6, wherein the number of surfaces is two.

9.-10. (Cancelled)

11. (Currently Amended) A capacitor comprising:

a multilayered capacitor having a pair of substantially rigid outer surfaces formed from barium titanate; and

a plurality of pads located on the pair of substantially rigid outer surfaces wherein at least two of the plurality of pads are capable of being coupled to a substrate using a solder bump, wherein the multilayered capacitor includes a number of parallel conductive layers and the number of pads are coupled to the number of parallel conductive layers through vias and wherein the number of conductive layers is greater than about 50.

12. (Original) The capacitor of claim 11, wherein the number of pads is greater than about 4000.

13.-29. (Cancelled)

30. (Previously Presented) The capacitor of claim 2, wherein at least one of the at least four conductive layers comprises platinum.

31. (Previously Presented) The capacitor of claim 3, wherein each of the at least four conductive layers comprises palladium.

32. (Previously Presented) The capacitor of claim 5, wherein each of the at least four conductive layers comprises tungsten.

33. (Previously Presented) The capacitor of claim 5, wherein each of the at least four conductive layers comprises palladium.

34. (Previously Presented) The capacitor of claim 11, wherein the dielectric includes at least two outer layers, each of the two outer layers having a thickness of about 7 microns.

35. (Currently Amended) The capacitor of claim 34, wherein ~~each of the at least four conductive layers~~ the number of conductive layers comprises tungsten.

36. (Currently Amended) The capacitor of claim 12, wherein ~~each of the at least four conductive layers~~ the number of conductive layers comprises platinum.

37. (Previously Presented) The capacitor of claim 36, wherein the dielectric includes at least two outer layers, each of the two outer layers having a thickness of about 7 microns.